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L#	Hits	Search String	Date Databases
L1	170	circuit$4 and rule$2 and violation$2 and (layout near10 view$6)	US-PGPUB; USPAT; EPO; JPO; DERWENT
L2	54	1 and (zoom$5 or magnif$8)	US-PGPUB; USPAT; EPO; JPO; DERWENT
L3	46	5325309.uref.	US-PGPUB; USPAT; EPO; JPO; DERWENT
L4	103	circuit$4 and ((defect$5 and layout) near10 view$6)	US-PGPUB; USPAT; EPO; JPO; DERWENT
L5	1559	circuit$4 and (design near10 layout) and view$6 and (violation$2 or defect$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT
L6	78	5 and view$6 near10 (violation$2 or defect$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT
L7	1	20010020194.PN.	US-PGPUB
L8	1	6507933.PN.	USPAT; USOCR
L9	1	6539272.PN.	USPAT; USOCR
L10	36	5896300	US-PGPUB; USPAT; EPO; JPO; DERWENT
L11	6	5896300.PN. or "6009252".pn. or "6115546".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT
L12	10	6009252.uref.	US-PGPUB; USPAT; EPO; JPO; DERWENT

Results of search set L4:

US 20040169850 A1	System and method for double sided optical inspection of thin film disks or wafers	20040902	356/237.2
US 20040155999 A1	Liquid crystal display device and electronic apparatus	20040812	349/114
US 20040134231 A1	Liquid crystal display unit-use glass substrate and method of producing mother glass and mother glass inspection device	20040715	65/29.11
US 20040121571 A1	Semiconductor device and a method of manufacturing the same	20040624	438/586
US 20040090566 A1	Thin film transistor array panel	20040513	349/43
US 20040086170 A1	Pattern inspecting method and apparatus thereof, and pattern inspecting method on basis of electron beam images and apparatus thereof	20040506	382/149
US 20040080938 A1	Uniform illumination system	20040429	362/231
US 20040055793 A1	Electromagnetic inductive system with multi-induction loop layout and battery less pointer device and its method for locating the coordinate	20040325	178/18.01
US 20040004879 A1	Semiconductor integrated circuit device	20040108	365/203
US 20030229865 A1	Method for eliminating false failures saved by redundant paths during circuit area analysis on an integrated circuit layout	20031211	716/4
US 20030205731 A1	Semiconductor integrated circuit device and manufacturing method thereof	20031106	257/200

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US 20030186490 A1	Semiconductor circuit and method of fabricating the same	20031002	438/166
US 20030184705 A1	Electro-optical apparatus having faces holding electro-optical material in between flattened by using concave recess, manufacturing method thereof, and electronic device using same	20031002	349/158
US 20030107039 A1	Thin Film Transistor Array Panel	20030612	257/72
US 20030071309 A1	Electro-optical apparatus, driving substrate for an electro-optical apparatus and method of manufacturing them	20030417	257/350
US 20030063792 A1	Apparatus for inspecting a specimen	20030403	382/149
US 20030062487 A1	Pattern inspection method and system therefor	20030403	250/492.2
US 20030050761 A1	Inspection method and its apparatus, inspection system	20030313	702/82
US 20030042289 A1	Electronic parts assembling and testing method, and electronic circuit baseboard manufactured by the method	20030306	228/103
US 20030007677 A1	Method and its apparatus for inspecting a pattern	20030109	382/149
US 20020173091 A1	Semiconductor integrated circuit device and manufacturing method thereof	20021121	438/200
US 20020170028 A1	Computer-aided layout design system with automatic defect-zooming function	20021114	716/11
US 20020153536 A1	Semiconductor device	20021024	257/197
US 20020149020 A1	Thin film transistor array panel	20021017	257/72
US 20020145683 A1	Electro-optical apparatus having faces holding electro-optical material in between flattened by using concave recess, manufacturing method thereof, and electronic device using same	20021010	349/43
US 20020051412 A1	Recording apparatus and recording method	20020502	369/47.39
US 20020028539 A1	Semiconductor device and method for fabricating the same	20020307	438/132
US 20010033683 A1	Method of inspecting a pattern and an apparatus thereof and a method of processing a specimen	20011025	382/149
US 20010033517 A1	Information storage medium, information recording method, and information reproduction method	20011025	365/200
US 20010032387 A1	Electric wiring forming system	20011025	29/740
US 20010024859 A1	Semiconductor integrated circuit device and a method of manufacturing thereof	20010927	438/286
US 20010020718 A1	Semiconductor integrated circuit device and a method of manufacturing thereof	20010913	257/326
US 20010019499 A1	Semiconductor integrated circuit device	20010906	365/182
US 6810510 B2	Method for eliminating false failures saved by redundant paths during circuit area analysis on an integrated circuit layout	20041026	716/5
US 6799130 B2	Inspection method and its apparatus, inspection system	20040928	702/82
US 6753253 B1	Method of making wiring and logic corrections on a semiconductor device by use of focused ion beams	20040622	438/676
US 6697037 B1	TFT LCD active data line repair	20040224	345/93

US 6671243 B2	Information storage medium, information recording method, and information reproduction method	20031230	369/59.1
US 6657231 B2	Thin film transistor array panel	20031202	257/72
US 6614923 B1	Pattern inspecting method and apparatus thereof, and pattern inspecting method on basis of electron beam images and apparatus thereof	20030902	382/149
US 6613500 B1	Reducing resist residue defects in open area on patterned wafer using trim mask	20030902	430/394
US 6611458 B2	Semiconductor integrated circuit device	20030826	365/185.09
US 6611301 B2	Electro-optical apparatus having faces holding electro-optical material in between flattened by using concave recess, manufacturing method thereof, and electronic device using same	20030826	349/43
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US 6504215 B1	Electro-optical apparatus having a display section and a peripheral driving circuit section	20030107	257/350
US 6502004 B1	Method and apparatus for extracting bridges from an integrated circuit layout	20021231	700/110
US 6451636 B1	Semiconductor device and display device having laser-annealed semiconductor element	20020917	438/166
US 6444514 B1	Semiconductor integrated circuit device and manufacturing method thereof	20020903	438/221
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US 6433841 B1	Electro-optical apparatus having faces holding electro-optical material in between flattened by using concave recess, manufacturing method thereof, and electronic device using same	20020813	349/43
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US 6420754 B2	Semiconductor integrated circuit device	20020716	257/326
US 6392258 B1	High speed heterojunction bipolar transistor, and RF power amplifier and mobile communication system using the same	20020521	257/197
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US 6333545 B1	Semiconductor device having blocking layer and fuses	20011225	257/529
US 6330975 B1	Combined code reader and digital camera using a common photodetector	20011218	235/472.01
US 6236615 B1	Semiconductor memory device having memory cell blocks different in data storage capacity without influence on peripheral circuits	20010522	365/230.03
US 6204122 B1	Methods of forming nonvolatile integrated circuit memory devices having high capacitive coupling ratios	20010320	438/257
US 6184947 B1	Thin film transistor matrix with repairable bus line	20010206	349/42

US 6172513 B1	Method for analyzing electrical contact between two conductive members of semiconductor device without destruction thereof	20010109	324/756
US 6150206 A	Methods of forming integrated circuit capacitors using trench isolation and planarization techniques	20001121	438/238
US 6144214 A	Method and apparatus for use in IDDQ integrated circuit testing	20001107	324/763
US 6137295 A	Method of detecting defect of integrated circuit and apparatus thereof	20001024	324/751
US 6061281 A	Redundancy method and semiconductor circuit	20000509	365/200
US 6020867 A	Display apparatus	20000201	345/87
US 5962867 A	Abatement of electron beam charging distortion during dimensional measurements of integrated circuit patterns with scanning electron microscopy by the utilization of specially designed test structures	19991005	257/48
US 5960256 A	Wafer layout of semiconductor device and manufacturing method thereof	19990928	438/14
US 5947051 A	Underwater self-propelled surface adhering robotically operated vehicle	19990907	114/313
US 5943073 A	Ink jet recording apparatus and method	19990824	347/48
US 5937290 A	Method of manufacturing semiconductor integrated circuit devices using phase shifting mask	19990810	438/238
US 5872386 A	Wafer layout of semiconductor device	19990216	257/443
US 5821523 A	Combined code reader and digital camera using a common photodetector	19981013	235/472.01
US 5801412 A	Semiconductor device having a capacitance element with excellent area efficiency	19980901	257/296
US 5798831 A	Defect inspecting apparatus and defect inspecting method	19980825	356/237.2
US 5773857 A	Semiconductor device having dummy wiring conductors for suppressing heat-treatment-induced shifting	19980630	257/211
US 5736863 A	Abatement of electron beam charging distortion during dimensional measurements of integrated circuit patterns with scanning electron microscopy by the utilization of specially designed test structures	19980407	324/765
US 5712684 A	Viewing apparatus with visual axis detector	19980127	348/341
US 5680207 A	Defect inspecting apparatus and defect inspecting method	19971021	356/237.3
US 5615163 A	Semiconductor memory device	19970325	365/230.03
US RE35423 E	Method and apparatus for performing automated circuit board solder quality inspections	19970114	378/58
US 5517457 A	Semiconductor memory device	19960514	365/230.03
US 5497381 A	Bitstream defect analysis method for integrated circuits	19960305	714/745
US 5477067 A	Semiconductor IC device having a RAM interposed between different logic sections and by-pass signal lines extending over the RAM for mutually connecting the logic sections	19951219	257/211
US 5309246 A	Technique for generating additional colors in a halftone color image through use of overlaid primary colored halftone dots of varying size	19940503	358/1.9

US 5243208 A	Semiconductor integrated circuit device having a gate array with a ram and by-pass signal lines which interconnect a logic section and I/O unit circuit of the gate array	19930907	257/211
US 5147742 A	Photomask and fabrication of the same	19920915	430/5
US 5103282 A	Semiconductor integrated circuit device having a gate array with a RAM and by-pass signal lines which interconnect a logic section and I/O unit circuit of the gate array	19920407	257/211
US 4959704 A	Semiconductor integrated circuit device	19900925	257/208
US 4809308 A	Method and apparatus for performing automated circuit board solder quality inspections	19890228	378/98.2
US 4569024 A	Process and installation for the treatment of rough sheets issuing from a rolling mill for flat products	19860204	700/171
US 4557125 A	Apparatus for on line, random sample, inspection of cold-formed blanks for threaded fasteners	19851210	72/18.6
US 4084896 A	Photoelectrophoretic web imaging apparatus	19780418	399/131
US 4049343 A	Combination imaging and grounding roller	19770920	399/131
US 4038677 A	Composite semiconductor unit and method	19770726	257/529
US 4006982 A	Photoelectrophoretic concurrent process cycling	19770208	399/131
US 3991992 A	Photoelectrophoretic web machine servo drive system	19761116	270/52.07
US 3989366 A	Photoelectrophoretic imaging apparatus having a device for increasing the friction force between webs	19761102	399/131
US 3985434 A	Photoelectrophoretic pigment discharging with A.C. corotron or U.V. illumination	19761012	399/131
US 3983479 A	Electrical defect monitor structure	19760928	324/537
US 3982710 A	Photoelectrophoretic web tension system	19760928	242/412.2
US 3981459 A	Photoelectrophoretic electrostatic tacking capstan web tension system	19760921	242/419.3

Results of search set L6:

US 20040133369 A1	Method and system for context-specific mask inspection	20040708	702/59
US 20040126003 A1	Pattern inspection apparatus	20040701	382/141
US 20040115541 A1	Mask defect inspecting method, semiconductor device manufacturing method, mask defect inspecting apparatus, defect influence map generating method, and computer program product	20040617	430/30
US 20040113647 A1	Built-in self test of MEMS	20040617	324/763
US 20040095573 A1	Excimer laser inspection system	20040520	356/237.5
US 20040091142 A1	Qualifying patterns, patterning processes, or patterning apparatus in the fabrication of microlithographic patterns	20040513	382/144

US 20040086791 A1	Photomask defect testing method, photomask manufacturing method and semiconductor integrated circuit manufacturing method	20040506	430/5
US 20040060018 A1	Defect tracking by utilizing real-time counters in network computing environments	20040325	716/4
US 20040057610 A1	Mask defect analysis for both horizontal and vertical processing effects	20040325	382/144
US 20040055793 A1	Electromagnetic inductive system with multi-induction loop layout and battery less pointer device and its method for locating the coordinate	20040325	178/18.01
US 20040015808 A1	System and method for providing defect printability analysis of photolithographic masks with job-based automation	20040122	716/19
US 20040009416 A1	Qualifying patterns, patterning processes, or patterning apparatus in the fabrication of microlithographic patterns	20040115	430/30
US 20030212969 A1	System and method for correcting charge collector violations	20031113	716/5
US 20030177455 A1	Method and apparatus for interconnect-driven optimization of integrated circuit design	20030918	716/2
US 20030138978 A1	Method for manufacturing semiconductor devices and method and its apparatus for processing detected defect data	20030724	438/5
US 20030126581 A1	User interface for a network-based mask defect printability analysis system	20030703	716/19
US 20030113009 A1	System and method for confirming electrical connection defects	20030619	382/147
US 20030097228 A1	Apparatus and methods for managing reliability of semiconductor devices	20030522	702/82
US 20030095699 A1	Method for applying a defect finder mark to a backend photomask making process	20030522	382/149
US 20030089614 A1	Tooling frame able to adhere to tin	20030515	205/125
US 20030054573 A1	Method for manufacturing semiconductor devices and method and its apparatus for processing detected defect data	20030320	438/4
US 20030050761 A1	Inspection method and its apparatus, inspection system	20030313	702/82
US 20030029345 A1	Ultra sensitive magnetic field sensors	20030213	102/221
US 20030022401 A1	Semiconductor device inspection method	20030130	438/14
US 20030009736 A1	Method and apparatus for detail routing using obstacle carving around terminals	20030109	716/8
US 20020170028 A1	Computer-aided layout design system with automatic defect-zooming function	20021114	716/11
US 20020164064 A1	System and method of providing mask quality control	20021107	382/145
US 20020152453 A1	Photomask and integrated circuit manufactured by automatically correcting design rule violations in a mask layout file	20021017	716/21
US 20020144230 A1	System and method for correcting design rule violations in a mask layout file	20021003	716/19
US 20020073869 A1	Ultra sensitive magnetic field sensors	20020620	102/221
US 20020052053 A1	Inspection system and semiconductor device manufacturing method	20020502	438/12
US 20020035461 A1	Visual analysis and verification system using advanced tools	20020321	703/13
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US 20010055085 A1	DISPLAY APPARATUS AND METHOD FOR MANUFACTURING THE SAME	20011227	349/139
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US 6797526 B2	Method for manufacturing semiconductor devices and method and its apparatus for processing detected defect data	20040928	438/5
US 6782524 B2	Photomask and integrated circuit manufactured by automatically correcting design rule violations in a mask layout file	20040824	716/19
US 6775817 B2	Inspection system and semiconductor device manufacturing method	20040810	716/21
US 6774957 B2	Display apparatus having an electric shielding wire and method for manufacturing the same	20040810	349/40
US 6757645 B2	Visual inspection and verification system	20040629	703/13
US 6753253 B1	Method of making wiring and logic corrections on a semiconductor device by use of focused ion beams	20040622	438/676
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US 6735750 B2	System and method for correcting charge collector violations	20040511	716/5
US 6629292 B1	Method for forming graphical images in semiconductor devices	20030930	716/3
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US 6357036 B1	Computerized method and apparatus for designing wire bond diagrams and locating bond pads for a semiconductor device	20020312	716/15

US 6249898 B1	Method and system for reliability analysis of CMOS VLSI circuits based on stage partitioning and node activities	20010619	716/4
US 6185707 B1	IC test software system for mapping logical functional test data of logic integrated circuits to physical representation	20010206	714/724
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US 5937290 A	Method of manufacturing semiconductor integrated circuit devices using phase shifting mask	19990810	438/238
US 5933522 A	Specific part searching method and device for memory LSI	19990803	382/149
US 5896299 A	Method and a system for fixing hold time violations in hierarchical designs	19990420	716/4
US 5781446 A	System and method for multi-constraint domain electronic system design mapping	19980714	716/9
US 5771321 A	Micromechanical optical switch and flat panel display	19980623	385/31
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US 5594800 A	Sound reproduction system having a matrix converter	19970114	381/20
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US 5103282 A	Semiconductor integrated circuit device having a gate array with a RAM and by-pass signal lines which interconnect a logic section and I/O unit circuit of the gate array	19920407	257/211
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US 4755874 A	Emission microscopy system	19880705	348/126
US 4721995 A	Integrated circuit semiconductor device formed on a wafer	19880126	257/777
US 3983479 A	Electrical defect monitor structure	19760928	324/537

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1 **Net ordering for timing and wiring optimization**
Selinger, C.R.; Schell, T.A.; Kleinman, Y.;
ASIC Conference and Exhibit, 1993. Proceedings., Sixth Annual IEEE International , 27 Sept.-1 Oct. 1993
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2 **Techniques for yield enhancement of VLSI adders**
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3 **A fault diagnosis methodology for the UltraSPARC™-I microprocessor**
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4 **A new approach to scan chain reordering using physical design information**
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5 **Three-dimensional defect sensitivity modeling for open circuits in ULSI structures**
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Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 17 Issue: 4 , April 1998
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[Abstract] [PDF Full-Text (168 KB)] **IEEE JNL**

6 **Yield estimation of VLSI circuits with downscaled layouts**
Pleskacz, W.A.;
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7 **SmartBit^{TM}: bitmap to defect correlation software for yield improvement**
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8 **An optimal replacement policy for cooling of 3D stacked mesh array**
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9 **A 3-step approach for performance-driven whole-chip routing**
Yih-Chih Chou; Youn-Long Lin;
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1 RISCE—a reduced instruction set circuit extractor for hierarchical VLSI layout verification

Volker Henkel, Ulrich Golze

June 1988 **Proceedings of the 25th ACM/IEEE conference on Design automation**

Full text available: pdf(1.00 MB) Additional Information: full citation, abstract, references, citings, index terms

We present a circuit extractor preserving the hierarchical layout structure isomorphically. As opposed to existing extractors, our approach permits all cell overlaps which are electrically meaningful. New mask operations based on stretched geometries handle topologically open and closed areas. A reduced set of model independent instructions is introduced for device recognition. An existing implementation is discussed.

2 An enhanced flow model for constraint handling in hierarchical multi-view design environments

Pieter van der Wolf, Olav ten Bosch, Alfred van der Hoeven

November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(958.27 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we present an enhanced design flow model that increases the capabilities of a CAD framework to support design activities on hierarchical multi-view design descriptions. This flow model offers new constructs for the configuration of complex design constraints in terms of conditions on the hierarchical multi-view structure of a design. The design flow management system enforces these constraints and uses them to inform the designer more effectively about the validity of verifica ...

3 Session 6A: placement II: Effective partition-driven placement with simultaneous level processing and global net views

Ke Zhong, Shantanu Dutt

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(113.97 KB) Additional Information: full citation, abstract, references, citings

In this paper we take a fresh look at the partition-driven placement (PDP) paradigm for standard-cell placement for wire-length minimization. The goal is to develop several new algorithms for incorporation into a PDP framework that can rectify the well-known drawbacks of traditional PDP (increasingly localized view of nets with increasing levels of the partitioning tree, min-cut objective, inaccuracy and cost of terminal propagation (TP), irreversibility of move decisions), while preserving its ...

4 Automatic layout synthesis of leaf cells

Sanjay Rekhi, J. Donald Trotter, Daniel H. Linder

January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**

Full text available: pdf(154.40 KB) Additional Information: full citation, references, citings, index terms

5 Highlights of CMU research on CAD, CAM and CAT of VLSI circuits

John Paul Shen

November 1999 **Proceedings of 1986 ACM Fall joint computer conference**

Full text available: pdf(1.35 MB) Additional Information: full citation, references, index terms

6 Technology retargeting for IC layout

John Lakos

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available: pdf(87.81 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

The ability to recognize polygon-based layout as a collection ofobjects representing circuit elements connected by path-based wires,enables existing designs implemented using an older fabricationprocess to be reimplanted quickly in a new process.The approachtaken here, based on layout generator technology, is to create acollection of parameterized circuit objects that, with appropriatearguments, are able to represent the devices (e.g., transistors,contacts) implicitly described in the flattened ...

7 Placement of variable size circuits on LSI masterslices

K. H. Khokhani, A. M. Patel, W. Ferguson, J. Sessa, D. Hatton

June 1981 **Proceedings of the 18th conference on Design automation**

Full text available: pdf(671.53 KB) Additional Information: full citation, abstract, references, citings, index terms

With the advent of large scale integration (LSI and VLSI), logic circuit densities per chip have grown to hundreds and thousands. The arrangement of interconnected logic circuits of different sizes and shapes poses a difficult combinatorial placement problem. In this paper, an overview of techniques is presented for placing different size rectangular circuits with limited locations on the chip, considering the function of level sensitive scan design (LSSD)1, as well as ...

8 Hierarchical Current Density Verification for Electromigration Analysis in Arbitrary Shaped Metallization Patterns of Analog Circuits

G. Jerke, J. Lienig

March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(367.21 KB) Publisher Site Additional Information: full citation, abstract

Electromigration is caused by high current density stressin metallization patterns and is a major source of break-down in electronic devices. It is therefore an importantreliability issue to verify current densities within allstressed metallization patterns. In this paper we propose anew methodology for hierarchical verification of currentdensities in arbitrarily shaped analog circuit layouts,including a quasi-3D model to verify irregularities suchas vias. Our approach incorporates thermal simul ...

9 A 2-dimensional placement algorithm for the layout of electrical circuits.

Daniel G. Schweikert

June 1976 **Proceedings of the 13th conference on Design automation**

Full text available: pdf(803.45 KB) Additional Information: full citation, abstract, references, citings, index terms

PLAC is a multi-algorithm, 2-dimensional placement program which accommodates many of the "real world" constraints which occur in the layout of electrical circuits. PLAC was implemented as part of LTX [1], a general integrated circuit layout system, but is capable of handling circuit layout tasks from other technologies (e.g., PC boards, ceramic substrates). PLAC interlaces constructive initial placement with iterative pairwise exchange, using an approximation of tota ...

10 A 2-dimensional placement algorithm for the layout of electrical circuits

D. G. Schweikert

June 1988 **Papers on Twenty-five years of electronic design automation**

Full text available: pdf(960.80 KB) Additional Information: full citation, references, index terms

11 Cellular image processing techniques for VLSI circuit layout validation and routing

T. N. Mudge, R. A. Rutenbar, R. M. Lougheed, D. E. Atkins

January 1982 **Proceedings of the 19th conference on Design automation**

Full text available: pdf(769.83 KB) Additional Information: full citation, abstract, references, citings, index terms

The architecture of the Cytocomputer?, an existing special-purpose, pipelined cellular image processor, is described. A formalism used to express cellular operations on images is then given. Cellular image processing algorithms are then developed that perform (1) design rule checks (DRC's) on VLSI circuit layouts, and (2) Lee-type wire routing. Two sets of cellular image processing transformations for checking the Mead and Conway design rules and for Lee-routing have been defined and used t ...

12 Automatic VLSI layout verification

Laurin Williams

June 1981 **Proceedings of the 18th conference on Design automation**

Full text available: pdf(468.70 KB) Additional Information: full citation, abstract, references, citings, index terms

Xerox has instituted a set of software tools that close the loop between circuit design and mask generation of VLSI and provide checks and analysis along the way. The software includes circuit extraction, capacitance calaulation, nodal analysis and logic recognition as well as interfaces to graphic systems. The systematic method of capturing circuit designs and the software packages for analyzing mask data are described in this paper. The kinds of errors checked and the method of reporting ...

13 Magic: A VLSI layout system

John K. Ousterhout, Gordon T. Hamachi, Robert N. Mayo, Walter S. Scott, George S. Taylor

June 1984 **Proceedings of the 21st conference on Design automation**

Full text available: pdf(825.95 KB) Additional Information: full citation, abstract, references, citings, index terms

Magic is a "smart" layout system for integrated circuits. The user interface is based on a new design style called logs, which combines the efficiency of mask-level design with the flexibility of symbolic design. The system incorporates expertise about design rules and connectivity directly into the layout system in order to implement powerful new operations, including: a continuous design-rule checker that operates in background to maintain an up-to-date pictur ...

14 The Compilation of Regular Expressions into Integrated Circuits

Robert W. Floyd, Jeffrey D. Ullman

July 1982 **Journal of the ACM (JACM)**, Volume 29 Issue 3

Full text available: pdf(983.18 KB) Additional Information: full citation, references, citings, index terms

15 A data path layout assembler for high performance DSP circuits

H. Cai, S. Note, P. Six, H. De Man

January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation**

Full text available: pdf(767.84 KB) Additional Information: full citation, abstract, references, citings, index terms

A system is presented which automatically generates layout of bit-sliced data paths in high performance DSP circuits. The system consists of a linear placement tool, a track assignment tool and detailed layout tools. In this paper we will present algorithms for linear placement of modules and routing track assignment across the modules. By taking advantage of the inherent structure of the circuits an A* based linear placement algorithm has produced better results compar ...

16 The role of timing verification in layout synthesis

Jacques Benkoski, Andrzej J. Strojwas

June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**

Full text available: pdf(889.07 KB) Additional Information: full citation, references, citings, index terms

17 Fabric-driven logic synthesis: River PLAs: a regular circuit structure

Fan Mo, Robert K. Brayton

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(297.44 KB) Additional Information: full citation, abstract, references, citings, index terms

A regular circuit structure called a River PLA and its re-configurable version, Glacier PLA, are presented. River PLAs provide greater regularity than circuits implemented with standard-cells. Conventional optimization stages such as technology mapping, placement and routing are eliminated. These two features make the River PLA a highly predictable structure. Glacier PLAs can be an alternative to FPGAs, but with a simpler and more efficient design methodology.

Keywords: programmable logic array, river routing

18 The evolution of design automation to meet the challanges of VLSI

Lawrence M. Rosenberg

June 1980 **Proceedings of the 17th conference on Design automation**

Full text available: pdf(997.27 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents the author's opinion of the major problems confronting Design Automation for VLSI and how Design Automation may evolve to meet these challenges. The paper first takes a historical look at the driving forces for Design Automation development by analyzing the evolution of Design Automation at RCA. It looks at both some successful and unsuccessful development efforts and attempts to isolate some of the criteria necessary for success. It review RCA's current LSI Design Autom ...

19 A "non-restrictive" artwork verification program for printed circuit boards

David Kaplan

January 1982 **Proceedings of the 19th conference on Design automation**

Full text available: pdf(639.01 KB) Additional Information: full citation, abstract, references, index terms

This paper describes a PCB artwork verification program which imposes virtually no restrictions on the layout designer. The program is capable of making fast and reliable verifications of layouts of any type and style. The concepts and techniques used to achieve the "non-restrictive" feature of the program are discussed. A unique characteristic of the program is the special treatment of nonelectrical elements. The program has been proven by continuous practical use in a dynamic ...

20 Session 8C: advances in layout and synthesis: Layout-driven area-constrained timing optimization by net buffering

Rajeev Murgai

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(252.73 KB) Additional Information: full citation, abstract, references

With the advent of deep sub-micron technologies, interconnect loads and delays are becoming significant, and layout-driven synthesis has become the need of the day. However, given the tight constraints imposed by the layout (e.g., area availability, congestion), only those synthesis transforms can be made layout-driven that are local and layout-friendly. Examples of such transforms are net buffering, gate resizing, and gate replication.In this paper, we address the problem of minimizing the dela ...

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